

Appl. No. 10/709,569  
Amdt. dated May 10, 2005  
Reply to Office action of March 11, 2005

REMARKS/ARGUMENTS

Claims 1-5, 7-12 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Norstrom et al (6,657,242). Claims 14-17, 20, 21 have been allowed.

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1. Rejection of claims 1-5, 7-12 under 35 U.S.C. 103(a):

Claims 1-5, 7-12 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Norstrom et al (6,657,242). For reasons of record that can be found on pages 2-3 in the Office action identified above, which is part of paper no/mail date 20050307.

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Response:

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According to claim 1 and Figs.7-14 of the present application, the bipolar junction transistor comprises a substrate 70, a dielectric layer 84 on the substrate 70, with an opening 98 that exposes a portion of the substrate 70, a heavily doped polysilicon layer 104 on the sidewall of the opening, an intrinsic base doped region 108 positioned in the bottom of the opening, a spacer 106 formed on the heavily doped polysilicon layer to defined a self-aligned emitter region in the opening, an emitter conductivity layer 105 being filled within the self-aligned emitter region, a PN junction being formed between the emitter conductivity layer and the intrinsic base doped region, and a selective implant collector region 102 located in a substrate. Therefore, the bipolar junction transistor of the present application comprises a collector 102 positioned beneath the emitter conductivity layer 105 and the intrinsic base doped region 108.

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Referring to the application of Norstrom et al., they only disclose to form a N+ collector 159 on the silicon substrate 100 and near the N+ emitter 143, but never teach to form a collector in the silicon substrate 100 and beneath the N+ emitter 143.

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Accordingly, the position of the collector N+ collector 159 of Norstrom et al. is different from the selective implant collector region 102 of the present application so that the bipolar structure of Norstrom et al. is different from the structure of the bipolar junction transistor of the present application. Therefore, the Applicant believes 5 that it is not obvious to derive the whole structure of the present application from Norstrom et al., and claim 1 of the present application should be patentable. Reconsideration of claim 1 is politely requested.

Claims 4-5 and 7-12 are dependent upon claim 1, thus they should be allowed if 10 claim 1 is allowed. Reconsideration of claims 4-5 and 7-12 are hereby requested.

**2. Allowance of claims 14-17, 20, 21:**

The Applicant acknowledges and appreciates the allowance of claims 14-17, 20,

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Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

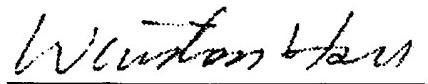
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Respectfully submitted,



Date: May 10, 2005

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